CLAIMS

1. A method of fabricating a memory device comprising:

providing a substrate;

forming a first n-type layer over the substrate;

forming a p-type layer over the first n-type layer;

forming a second n-type layer over the p-type layer;

forming a floating gate over the substrate;

etching a trench in the p-type layer of said memory device; and

forming a select gate in the trench, wherein said memory device defines a square feature size of $2F^2$.

2. The method of claim 1, wherein forming a first n-type layer over the substrate comprises forming a buried source over the substrate.

3. The method of claim 1, wherein forming a first p-type layer over the first n-type layer comprises forming a first p-type layer over the first n-type layer using epitaxial deposition.

4. The method of claim 1, forming a p-type layer over the first n-type layer comprises forming a vertical channel over the first n-type layer.

5. A method of fabricating a buried source comprising:

providing a wafer having a substrate;

covering a periphery of a wafer using an array mask;

doping source areas with a dopant; and

performing an epitaxial deposition to form a p-type channel, wherein performing an epitaxial deposition to form a p-type channel comprises performing an epitaxial deposition to

form a p-type channel to a determined thickness, wherein the thickness determines a channel length.

6. The method of claim 5, wherein doping source areas with a dopant comprises doping source areas with As.

7. The method of claim 5, wherein doping source areas with a dopant comprises doping source areas with Sb.

8. A method of fabricating a memory device comprising:

providing a wafer having a substrate;

forming a buried source in the substrate;

forming a vertical channel over the buried source;

performing a cell implant;

forming a tunnel oxide layer over the substrate;

forming a first poly layer over the tunnel oxide layer;

forming a nitride layer over the first poly layer;

patterning wordlines into the memory device, wherein the memory device defines a square feature size of less than $4F^2$;

forming STI areas in the memory device;

removing the nitride layer; and

forming an oxide nitride oxide layer over a surface of the memory device.

9. The method of claim 8, wherein forming STI areas in the memory device further comprises etching the nitride layer and etching the first poly layer.

10. The method of claim 8, wherein forming STI areas in the memory device further comprises depositing a STI oxide over the STI areas and filling the STI areas with a field oxide.

11. The method of claim 8, further comprising:

polishing a surface of the memory device using chemical mechanical polishing to make the surface planar.

12. A method of fabricating a memory device comprising:

providing a wafer having a substrate;

forming a buried source over the substrate;

forming a vertical channel over the buried source;

forming a STI area and a self aligned floating gate;

depositing a BPSG layer over the substrate;

depositing a hardmask layer over the BPSG layer;

patterning active areas to form an active trench;

forming first spacers along sidewalls of the active trench;

forming a drain in the active trench; and

forming a wordline over the drain, wherein said memory device defines a square feature size of less than $4F^2$.

13. The method of claim 12, further comprising performing RTP on the memory device and polishing the surface of the memory device prior to depositing a hardmask layer.

14. The method of claim 12, wherein patterning active areas further comprises etching through the hardmask layer, the BPSG layer, an oxide nitride oxide layer and a first poly layer.

15. The method of claim 12, wherein forming first spacers comprises depositing a first spacer layer and etching the first spacer layer thereby leaving the first spacers along the sidewalls of the active trench.

16. The method of claim 12, further comprising:

forming a TiN layer over the active trench; and

forming a TiSi layer over the active trench.

17. The method of claim 12 further comprising:

performing a RTP on the memory device prior to forming a wordline.

18. The method of claim 12, wherein forming a wordline comprises:

depositing a wordline layer over the active trench;

polishing the wordline layer such that the wordline layer is planar to the hardmask layer; and

removing a portion of the wordline layer such that a lower portion of the wordline layer remains.

19. The method of claim 18, wherein removing a portion of the wordline layer comprises removing substantially half of the wordline layer.

20. The method of claim 12, further comprising depositing a second spacers over the wordline.

21. A method of fabricating a memory device comprising:

forming active areas in a substrate;

forming a floating gate layer over the substrate;

patterning rowlines in the memory device;

forming a removable spacer over the rowlines; and

etching a select trench in the substrate, wherein the memory cell defines a square feature size of about $2F^2$.

22. The method of claim 21 further comprising:

removing the removable spacer;

forming a select transistor oxide layer over the select trench;

forming a second poly layer over the surface of the memory device;

forming a conductive layer over the second poly layer; and

patterning the second poly layer and the conductive layer.

23. The method of claim 22, wherein forming a conductive layer over the second layer comprises forming a WSi_x layer over the second poly layer.

24. The method of claim 22, wherein forming a second poly layer over the surface of the memory device further comprises forming the second poly layer in the select trench to form a select gate.

25. A method of forming a memory device comprising:

forming a buried source formed in a substrate;

forming a first layer over said substrate;

forming a first drain formed in said first layer so as to define a first substantially vertical channel between said first drain and said buried source;

forming a trench in said first layer;

forming a select gate in said trench; and

forming a horizontal first floating gate over said first layer adjacent to said trench and proximate to said first substantially vertical channel, wherein said first floating gate is

dimensioned so as to define a sublithographic gate and the square feature size of the memory cell is not greater than $2F^2$.

26. The method of forming a memory device according to claim 25, further comprising:

forming a second drain formed in the first layer so as to define a second substantially vertical channel between said second drain and said buried source; and

forming a second floating gate over the first layer adjacent to the trench and proximate to the second substantially vertical channel.

27. The method of forming a memory device according to claim 25, wherein the floating gate is formed such that at least a portion of the floating gate overlies at least a portion of the drain.

28. The method of forming a memory device according to claim 25, wherein said trench is formed such that it extends through the first layer to the buried source.

29. The method of claim 25, wherein said formation of said source comprises forming a n-type layer over a substrate.

30. The method of claim 25, wherein said formation of said drain comprises forming a n-type layer over the source.

31. The method of claim 25, wherein said formation of said floating gate layer comprises:

forming a tunnel oxide layer;

forming a polysilicon layer over the tunnel oxide layer; and

forming an oxide layer over the polysilicon layer.

32. The method of claim 25, wherein said formation of said select gate comprises:

forming an oxide layer in the select trench; and

filling the select trench with polysilicon.

33. A method of forming a memory device comprising:

forming a first layer defining a source;

forming a second layer over the first layer;

forming a drain in the second layer so as to define a substantially vertical channel between said source and said drain;

forming a trench in the second layer;

forming a select gate in the trench; and

forming a horizontal floating gate over the second layer adjacent to the trench so as to avoid extending vertically down into the trench below the second layer, wherein the floating gate is dimensioned so as to define a sublithographic gate and the square feature size of the memory cell is not greater than $2F^2$.

34. The method of forming a memory device according to claim 33, wherein the trench is formed so as to extend through the second layer and into the first layer.

35. A computer system comprising at least one processor, a system bus, and a memory device coupled to the system bus, the memory device including at least one memory cell comprising:

a source;

a substantially vertical channel formed over the source;

a drain formed over the vertical channel; and

a substantially horizontal floating gate formed over at least a portion of the drain, wherein the square feature size of the memory cell is not greater than $2F^2$.